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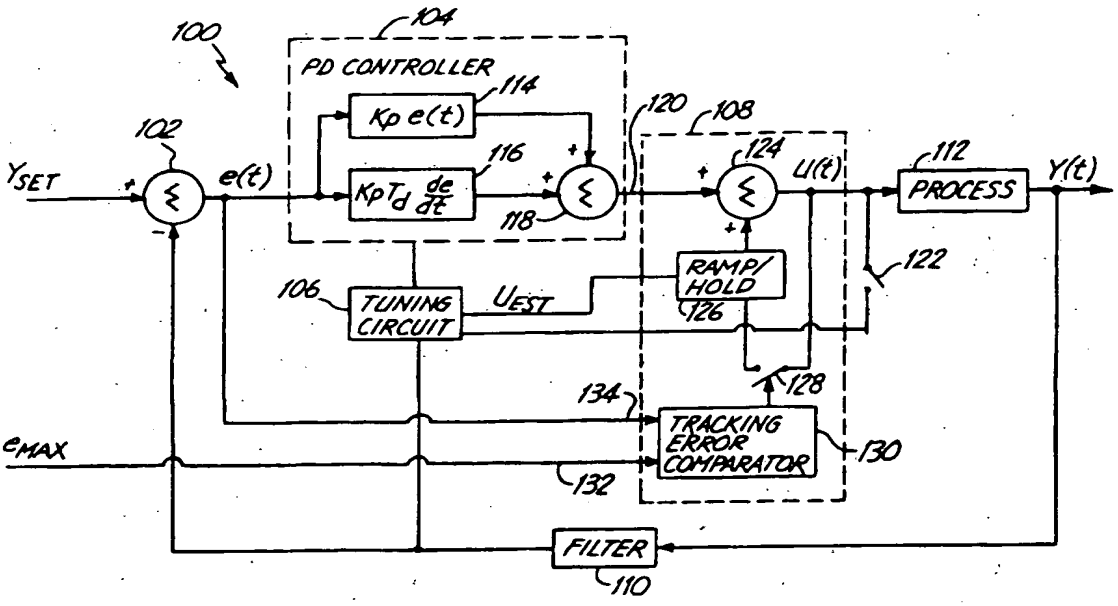

(57) Abstract

A process controller (100) controls an integrating-type process (112) based on a measured process variable (y(t)) and a set point (Y_{SET}). The process controller (100) includes an error generating circuit (102), a non-integrating control circuit (104) and an adaptive bias circuit (108). The error generating circuit (102) generates an error signal (e(t)) based on a difference between the set point (Y_{SET}) and the measured process variable (y(t)). The control circuit (104) generates a control signal (u(t)) as a function of the error signal (e(t)). The adaptive bias circuit (108) adds a bias value to the control signal (u(t)), the measured process variable (y(t)) or the set point (Y_{SET}). The bias value is selectively updated as a function of the error signal (e(t)) to force the error signal (e(t)) toward zero.

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ADAPTIVE BIAS CONTROLLER

BACKGROUND OF THE INVENTION

The present invention relates to an industrial process controller with adaptive bias, which can be implemented in low power and memory applications, such as in field mounted control units.

Field mounted control units include various devices, such as transmitters, actuators, transducers, switches and stand-alone controllers. Field mounted control units are used in process control systems to control the process, measure process variables and to generate outputs representative of the process variables for communication to central controllers or field control elements (e.g. values) over process control loops. The loops have included two-wire, three-wire and four-wire process control loops. Other loops have also been used, such as optical and radio frequency control loops.

Field mounted control units are mounted in a field area where current and voltage levels are typically limited to provide intrinsic safety. The units are often powered over the control loop. A separate transducer senses each process variable and provides the sensed variable to a transmitter for transmission to the central controller. Controllers can be located in a central control room or in the field and monitor the transducer outputs to generate appropriate control output signals. Control output signals are typically sent over a separate control loop to remote actuators, such as valves, which control the process according to the control output signals. In certain applications, controllers select the most appropriate set of instructions for process control equipment.

In one application, the transmitter itself includes a control function which provides the control output signals to the remote devices directly, thereby bypassing the central controller. A control function can also be located in the other field control elements, such as valves. This type of control unit is referred to as a field mounted control unit and is disclosed in more detail in Warrior et al., U.S. Patent No. 5,333,114, which is hereby incorporated by reference.

The control algorithm or equation performed by the controller in the transmitter or in the central control room is specially tailored to the process in which the controller is used. Several basic control algorithms exist, including Proportional (P), Proportional-Integral (PI) Proportional-Derivative (PD) and Proportional-Integral-Derivative (PID) control algorithms. The performance of the control algorithm is determined by control parameters, such as K_P, T_I and T_D which correspond to the proportional gain, integral time and derivative time, respectively, for an ideal-type of PID control algorithm. In some applications, K_P is replaced with a proportional band parameter PB, which is a function of K_P. Other types of PID control algorithms exist, such as parallel and serial equations. These algorithms have corresponding parameters which are similar to the ideal-type parameters. The control parameters are tuned based on a model of the underlying process to operate the process optimally.

SUMMARY OF THE INVENTION

A process controller controls an integrating-type process, such as a level process or flow control with a pulse duration output, based on a measured process variable and a set point. The process controller includes an error generating circuit, a non-

integrating control circuit and an adaptive bias circuit. The error generating circuit generates an error signal based on a difference between the set point and the measured process variable. The control circuit generates a first control signal as a function of the error signal. The adaptive bias circuit adds a bias value to the control signal, the measured process variable or the set point. The bias value is selectively updated as a function of the error signal to force the error signal toward zero.

In one embodiment, the bias value is added to the first control signal to generate a second control signal which is used to control the process. The bias value is selectively updated to equal a steady state level of the second control signal when the error signal exceeds a selected maximum error band. The updated bias value forces the error signal toward a predefined error band such that the measured process variable closely tracks the set point.

In another embodiment, the bias value is added in the error generation circuit such that the error signal is the sum of the measured process variable, the set point and the bias value. The bias value is selectively updated to equal this error signal at a steady state when the difference between the set point and the process variable is outside the predefined error band.

The adaptive bias circuit provides a tracking feature in the controller without the use of an integration term. This eliminates undesirable limit cycling caused by a double integration which occurs when an integration term is used with an integrating-type process.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a diagram of a level control system according to one embodiment of the present invention.

Figure 2 is a block diagram of a transmitter shown in Figure 1, which includes an adaptive bias controller according to the present invention.

Figure 3 is a diagram of the adaptive bias controller.

Figure 4 is flow chart which illustrates a procedure for updating a bias value in the adaptive bias controller.

Figure 5 is a waveform diagram illustrating an auto-tuning stage and a closed-loop adaptive bias control stage according to the present invention.

Figure 6 is a block diagram of a valve having an adaptive bias control unit according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention is an adaptive bias process control system which is computationally simple such that the system can be implemented in a low-power field-mounted control unit in a process control system. The control system performs a closed loop, non-integrating control function over the process through a control output signal as a function of predefined control parameters. An adaptive bias circuit adds a bias value to the control output signal which is updated when a difference between the measured process variable and a user defined set point exceeds a maximum error tolerance band.

Figure 1 is a diagram of one embodiment in which the process control system of the present invention is useful. The process control system

includes master controller 10, transmitter 12, tank 14, input valve 16 and output valve 18. Master controller 10 is coupled to transmitter 12 and input valve 16 through two-wire process control loop 20. Loop 20 can include a 4-20 mA or a 10-50 mA current loop, for example, which allows master controller 10, transmitter 12 and valve 16 to communicate with one another by varying the current level through the loop. In an alternative embodiment, master controller 10, transmitter 12 and valve 16 communicate by varying the voltage level on loop 20. Concurrently, master controller 10 and transmitter 12 communicate digitally over loop 20 in a carrier modulated fashion, such as in the HART® protocol.

Other digital communication systems can be used, including a Fieldbus Standard which is presently being adopted by the Fieldbus Foundation and a MODBUS Standard. Alternatively, loop 20 carries baseband modulated digital signals such as DE protocol. In addition, master controller 10 and transmitter 12 can communicate with one another optically over single or dual optical fibers or by radio frequency. An example of an optical control circuit is disclosed in U.S. Patent No. 5,258,868, which is hereby incorporated by reference.

Master controller 10 includes a controller 22 and a power source 23 which provide power and control to loop 20. Master controller 10 can be positioned in a central control room or in a remote, field location with transmitter 12. Master controller 10, transmitter 12 and valve 16 can be coupled to one another in a variety of configurations as discussed in more detail in Warrior et al., U.S. Patent No. 5,333,114.

In the embodiment shown in Figure 1, the magnitude of current flowing through loop 12 represents a control output u(t) which controls flow into tank 14 by controlling the position of valve 16. Transmitter 12 preferably includes its own control function which is capable of taking over the operation of loop 20 from master controller 10 and sinking a variable amount of current to adjust control output u(t). The position of valve 18 controls the flow out of tank 14. Valve 18 is adjusted by a valve control signal o(t) which is provided by a transmitter 26 over a two-wire process control loop 28 which can be coupled to loop 20 in parallel (as shown in phantom) with loop 20 in a cascade fashion. The parallel configuration is referred to as a multidrop configuration. The valve control signal o(t) can also be provided by a separate loop which is coupled to transmitter 12 or master controller 10.

A sensor 24 is coupled to tank 14 for measuring a level y(t) of fluid in the tank. The rate-of-change in level dy(t)/dt is a function of the positions of valves 16 and 18. The process in this example is a "direct action" process since an increase in u(t) causes an increase in y(t). In a "reverse action" process, an increase in u(t) would cause a decrease in y(t). Sensor 24 can include any suitable sensor, such as an absolute or differential pressure sensor, an ultrasonic sensor or a microwave sensor. Other types of sensors capable of generating a signal representative of the level of fluid in tank 14 can also be used.

The level control system shown in Figure 1 is one example of a non-self-regulating process. The present invention can also be used with other non-self-regulating processes, such as a flow control with a

pulse duration output. A non-self-regulating process is a process in which the measured process variable y(t) will continue to increase or decrease as long as the control signal u(t) is not equal to a steady state value U_{ss} (i.e., when the inlet and outlet flows are not equal in a level process). The mass balance equation of the level process shown in Figure 1 can be written as:

$$\frac{dy(t)}{dt} = m_1 u(t-L) - m_2 o(t) \qquad \text{Eq. 1}$$

The above equation assumes that valves 16 and 18 are linear and neglects a head pressure effect on the valves. L is the overall process dead time, t is time and m_1 and m_2 are constants corresponding to the volume flow into and out of tank 14 divided by the area of tank 14. By assuming o(t) is constant, the following general equation for a direct acting integral-type process can be derived from Equation 1:

$$\frac{dy(t)}{dt} = m_1 (u(t-L) - U_{ss}) \qquad \text{Eq. 2}$$

where U_{ss} is a steady state value of control output u(t).

Figure 2 is a block diagram of transmitter 12 according to a first preferred embodiment of the present invention. Transmitter 12 includes a rugged, explosion proof housing 34 for mounting in the field, input terminal 36, output terminal 38, input-output circuit 40, demodulator 42, digital-to-analog (D/A) converter 44, modulator 46, microprocessor 48, analog-to-digital (A/D) converter 50, process variable sensor 52, clock circuit 54 and memory 56. Clock circuit 54 is connected to microprocessor 48 to sequence the operation of the microprocessor.

Input terminal 36 is coupled to master controller 10 (shown in Figure 1) while output terminal 38 is coupled to valve 16 (also shown in Figure 1). Input-output circuit 40 is coupled between input terminal 36 and output terminal 38. Circuit 40 includes input filter circuit 70, voltage regulator 72, current sink 74 and current sink 76 which are connected in series with one another in loop 20. Input-output circuit 40 receives process signals from loop 20 at input terminal 36 and supplies control output signals u(t) at output terminal 38 as a function of the process signals. Voltage regulator 72 within input-output circuit 40 receives power from loop 20 and provides a regulated voltage for powering all the various elements of transmitter 12.

The process signals used in generating control output u(t) comprise set points representative of a desired process state, process variables produced by the process, commands and whole or partial instruction sets for operating microprocessor 48, coefficients of terms for controlling microprocessor 48 and status requests from master controller 10. Input filter circuit 70 receives the process signals and directs the signals to demodulator 42. Demodulator 42 demodulates modulated process signals from the current loop and provides corresponding digital information to microprocessor 48. The information can be stored in memory 56 if desired.

Microprocessor 48 also receives process signals from process variable sensor 52. Sensor 52 measures a process variable y(t) and provides the measurement to A/D converter 50 which digitizes the measurement for microprocessor 48. The process variable measurements can then be stored in memory 56 for analysis or transmitted back to master controller 10

over loop 20. Microprocessor 48 transmits digital information to master controller 10 through modulator 46 and current sink 76, which modulate the information onto loop 20. In an alternative embodiment, sensor 52 and A/D converter 50 are located external to transmitter 12. In this embodiment, the process variable measured by sensor 52 is communicated to microprocessor 48 over loop 20 along with other process variables from different sensors.

Current sink 74 adjusts control output u(t) by adjusting the level of current flowing through loop 20. Microprocessor 48 operates current sink 74 through D/A converter 44 based on a control algorithm or software routine stored in memory 56 and as a function of the measured process variable y(t), stored control parameters and instructions received from master controller 10. For example, master controller 10 may provide a set point Y_{SET} or other command to microprocessor 48 which instructs the microprocessor to adjust control output u(t) such that the process variable y(t) approaches the set point Y_{SET}.

Memory 56 may also include an auto-tuning algorithm or software routine which tunes the stored control parameters used by the control algorithm to achieve a desired control performance. The auto-tuning algorithm causes microprocessor 48 to adjust control output u(t) over time and observe a response in the process variable y(t). From this response, microprocessor 48 estimates model parameters, such as an estimated steady state control output value U_{EST}, the system dead time L and the constant m_1, and use the model parameters to calculate the desired control parameters for the control function. Although any tuning circuit or method can be used with the present

invention, examples of suitable tuning circuits and methods can be found in a co-pending application of Zou et al., entitled "Field Based Process Control Unit With Auto-Tuning," and filed on August 15, 1995, which is hereby incorporated by reference.

Several well-known control functions are available, such as P, PI, PD and PID control functions. The basic control equation for a PID controller in an ideal form is,

$$u(t) = K_P e(t) + \frac{K_P}{T_I}\int e(t)\,dt + K_P T_D \frac{de(t)}{dt} \qquad \text{Eq. 3}$$

where K_P, T_I and T_D are control parameters representing the proportional gain, integral time and derivative time, respectively.

In some applications, such as integrating processes, P or PD control functions may be preferred over PI and PID control functions. With an integrating process, the closed loop control performance of PI and PID control functions may experience undesirable limit cycling in the presence of valve hysteresis and friction due to double integration since the process acts as a natural integrator. Limit cycling occurs as the process variable oscillates about the set point, which causes the control signal and thus the control valve also to oscillate in an opposite direction to counteract oscillations in the process variable. There is no stable state in the process variable or the control signal. This compromises process quality, causes increased valve wear and affects upstream and downstream process. Although tuning the control parameters K_P, T_I and T_D can temporarily compensate for hysteresis and friction in a valve for a level control application,

limit cycling may reappear with changes caused by valve packing friction, for example.

The present invention reduces limit cycling by replacing the integration term in Equation 3 with a reset or bias value U_{RS}, as shown in the following equation,

$$u(t) = K_P e(t) + K_P T_D \frac{de(t)}{dt} + U_{RS} \qquad \text{Eq. 4}$$

Bias value U_{RS} is adaptively updated during normal closed loop control to minimize a tracking error introduced by a lack of integration

Figure 3 is an illustration of an adaptive bias process control system according to one embodiment of the present invention. The control and tuning algorithms stored in memory 56 configure microprocessor 48 as a process control system. Control system 100 includes summing junction 102, PD controller 104, tuning circuit 106, adaptive bias circuit 108, and filter 110, which are coupled to process 112. In one embodiment, the functions of these elements are performed by microprocessor 48 (shown in Figure 2). Although a PD type controller is shown in Figure 1, the present invention is also useful with a P type controller or a P(D) type controller where the D term is zero.

For a "direct action" process, a process variable set point Y_{SET} is provided to a positive input of summing junction 102 and the measured process variable y(t) is provided to a negative input of summing junction 102, through filter 110. For a "reverse action" process (not shown), Y_{SET} is provided to the negative input of summing junction 102 and y(t) is provided to the positive input of summing junction 102.

The output of summing junction 102 generates an error signal e(t) which represents a difference

between the set point Y_{SET} and the measured process variable y(t). Error signal e(t) is provided to PD controller 104. PD controller 104 includes proportional gain control block 114, derivative block 116 and summing junction 118. The outputs of blocks 114 and 116 are provided to positive inputs of summing junction 118. Summing junction 118 generates a first control output signal on output 120 that is combined with a bias value U_{RS} to generate a second control output signal u(t) which controls process 112.

In one embodiment, the control parameters K_P and T_D of blocks 114 and 116 may be tuned, or modified by tuning circuit 106 to match the characteristics of process 112 and to obtain a desired control performance. Tuning circuit 106 provides an open loop excitation signal, which varies over time, to process 112 through switching junction 122. The excitation signal provided by tuning circuit 106 is used as the second control output signal u(t) for disturbing process 112 during an auto-tuning stage. Switching junction 122 can be an actual switch or can be a transfer of control from one algorithm or software routine to the next. Tuning circuit 106 then observes the response in the measured process variable y(t) through filter 110 and generates a model of process 112.

As disclosed in the co-pending Zou et al. application, the process model parameters U_{EST}, m_1 and L may be estimated from the response in y(t) as:

$$U_{EST} = \frac{R_R U_{MIN} + R_F U_{MAX}}{R_R + R_F}$$

$$m_1 = \frac{R_R}{U_{MAX} - U_{EST}} = \frac{R_F}{U_{EST} - U_{MIN}} = \frac{R_R + R_F}{U_{MAX} - U_{MIN}} \qquad \text{Eqs. 5-7}$$

$$L = \max(L_R, L_F)$$

where R_R and R_F are the rising and falling rates of change in the measured process variable y(t), L_R and L_F are the rising and falling system dead times, and U_{MAX} and U_{MIN} are sequential maximum and minimum control signal disturbances applied to process 112 through switching junction 122. The process model parameters are then used to tune the control parameters K_P and T_D. Equations 5-7 are easily modified to estimate a process in which the process is reverse acting by exchanging U_{MAX} and U_{MIN}. Other process model estimation equations can also be used with the present invention. Once the model has been estimated, any suitable set of tuning rules can be used to tune the parameters, such as internal model-based control (IMC) and Lambda tuning rules. The process model and tuned control parameters are then stored in memory 56 (Figure 2) and can be provided to master controller 10 over process control loop 36.

Adaptive bias control circuit 108 is coupled between P or PD controller 104 and process 112. Circuit 108 includes summing junction 124, ramp and hold circuit 126, switching junction 128 and tracking error comparator circuit 130. Summing junction 124 has one positive input coupled to the output of summing junction 118 and another positive input coupled to ramp and hold circuit 126. Summing junction 124 generates the second control output signal u(t) which is the sum of the first control output signal 120 of PD controller 104 and bias reset value U_{RS} provided by ramp and hold circuit 126. Control output signal u(t) is fed back to ramp and hold circuit 126 through switching junction 128. Tracking error comparator circuit 130 controls the state of switching junction 128 as a function of a comparison of a maximum tracking error e_{MAX} provided at input 132 and the tracking error signal e(t) provided at input 134.

The value of e_{MAX} may be selected by the user and can be provided by master controller 10 (Figure 1) over loop 20 for storage in memory 56 (Figure 2).

Summing Junction 124 represents the addition of bias reset value U_{RS} in Equation 4. Since the differential equation defined by Equations 2 and 4 has a solution at the stable state, $y(t) = Y_{SS}$, $u(t) = U_{SS}$, $e(t) = e_{SS}$ and $de(t)/dt = 0$. Therefore,

$$e_{SS} = \frac{U_{SS} - U_{RS}}{K_P} \qquad \text{Eq. 8}$$

The tracking error is inversely proportional to K_p, and directly proportional to the difference U_{SS}-U_{RS}. If the bias reset value U_{RS} is selected so that $U_{RS} = U_{SS}$, the stable state tracking error $e(t) = e_{SS}$ will approach zero.

Given Equation 8, tracking error comparator circuit 130 operates switching junction 128 according to the flow chart shown in Figure 4. When process control system 100 begins closed loop control of process 112, switching junction 122 opens. The process model has been estimated and the control function parameters have been calculated. At step 140, tuning circuit 106 provides the estimated steady state control output value U_{EST} to ramp and hold circuit 126 which ramps U_{RS} to U_{EST} for initializing the control output $u(t)$. The estimated value U_{EST} may be somewhat different from the real U_{SS}. Consequently, PD controller 104 receives a tracking error $e(t)$ from summing junction 102. At step 142, tracking error comparator circuit 130 waits a user-defined time period to allow $y(t)$ and $e(t)$ to approach a stable state. The time period may be any period such as several seconds or minutes.

After waiting the selected time period, tracking error comparator 130 begins observing samples of error e(t) and compares the samples with the maximum tracking error value e_{MAX}, at step 144. If |e(t)| is less than e_{MAX}, no action is necessary and tracking error comparator circuit 130 leaves switching junction 128 open such that bias value U_{RS} is not updated. If |e(t)| is greater than e_{MAX}, then tracking error comparator circuit 130 verifies whether the process is stable.

There are several ways in which tracking error comparator circuit 130 can verify whether the process is stable. In one embodiment, N samples of error e(t) are collected, at step 146, which are fit into a curve an+b with a least square data fitting method where a is the slope, n is the sample and b is the intercept. Specifically,

$$\begin{aligned} a \cdot 1 + b &= e(1) \\ a \cdot 2 + b &= e(2) \\ &\vdots \\ a \cdot N + b &= e(N) \end{aligned} \qquad \text{Eq. 9}$$

The above equation can be written in the following matrix form,

$$\begin{bmatrix} 1 & 1 \\ 2 & 1 \\ \dots & \dots \\ N & 1 \end{bmatrix} \begin{bmatrix} a \\ b \end{bmatrix} = \begin{bmatrix} e(1) \\ e(2) \\ \dots \\ e(N) \end{bmatrix} \qquad \text{Eq. 10}$$

This equation is solved according to the least square data fitting method by modifying the equation by the following matrix,

$$\begin{bmatrix} 1 & 2 & \dots & N \\ 1 & 1 & \dots & 1 \end{bmatrix} \qquad \text{Eq. 11}$$

which results in

$$\begin{bmatrix} \sum n^2 & \sum n \\ \sum n & \sum 1 \end{bmatrix} \begin{bmatrix} a \\ b \end{bmatrix} - \begin{bmatrix} \sum ne(n) \\ \sum e(N) \end{bmatrix} \qquad \text{Eq. 12}$$

By inverting the left matrix and reorganizing the equation, the equation becomes:

$$\begin{bmatrix} a \\ b \end{bmatrix} - \frac{12}{N(N^2-1)} \begin{bmatrix} \sum ne(n) - \frac{1}{2}(N+1)\sum e(n) \\ -\frac{1}{2}(N+1)\sum ne(n) + \frac{1}{6}(N+1)(2N+1)\sum e(n) \end{bmatrix} \qquad \text{Eq. 13}$$

The terms a and b are calculated, at step 146, according to the above equation. These terms can be calculated by simply calculating the terms $\Sigma e(n)$ and $\Sigma ne(n)$. Once a and b are determined, tracking error comparator circuit 146 determines whether the process is stable. If the slope $|a|$ of the curve is less than a threshold value a_{MAX}, at step 148, the process is stable and is outside the allowed error band (determined at step 144). The threshold value a_{MAX} may represent a specified change in level over a specified period of time, for example. The bias reset value U_{RS} is updated, at step 150, to equal the present value of u(t) so that the stable state error function e_{SS} will approach zero.

In some applications, such as averaging level process control, a sudden change or "bump" in the control signal u(t) will upset the upstream or downstream process. Therefore, a "bumpless" update of bias value U_{RS} is often desired. This can be achieved with a linear or exponential ramp function to smooth the bias value and thus the control signal update. In one example,

$$\begin{aligned} newU_{RS} &= oldU_{RS} + Rt \quad if\ 0 \le t \le T \\ newU_{RS} &= U_{SS} \quad if\ t > T \end{aligned} \qquad \text{Eq. 14}$$

where,

$$R = \frac{U_{SS} - oldU_{RS}}{T} \qquad \text{Eq. 15}$$

R is the rate of the ramp and T is the ramp period. In another example,

$$newU_{RS} = U_{SS} + (oldU_{RS} - U_{SS})\exp(-Rt) \qquad \text{Eq. 16}$$

where R is the time constant of the exponential ramp function.

If the slope |a| of the curve is greater than the threshold value a_{MAX}, then tracking error comparator circuit 130 determines whether the product, ab, is less than zero, at step 152. If so, a>0 and b<0 or a<0 and b>0, which means that the error e(t) is approaching the error band. There is no need to take any action in this case and tracking error comparator circuit 130 returns to wait step 142.

If ab>0, the error e(t) is outside the allowed band and the process variable y(t) is moving away from the set point. In this situation, action is required to bring the process variable y(t) toward the set point to avoid possible limit cycling in the load (or demand) where there never exists a stable control state, such as when cascade tanks experience load limit cycling. At step 154, a small offset, $K_I b$, is added to bias value U_{RS}, where K_I is a user-defined integral gain constant that is stored in memory 56. The offset brings the process variable y(t) back toward the set point. Tracking error comparator 130 then returns to wait step 142. This process is repeated periodically to adapt bias value U_{RS} to load and disturbance changes.

Several other ways to determine whether the process is stable exist and can be used with the present invention. For example, a more simplified method

involves collecting N samples of the error e(t) and determining whether the statistical variance of the samples is smaller than a threshold value. If so, then the process is stable. Since the process is stable, and the error is outside the error band, as determined at step 144, the bias value U_{RS} is updated with a ramp transition to equal the present value of u(t).

Figure 5 is a waveform diagram which illustrates the adaptive bias operation. Waveform 180 represents the magnitude of the control output u(t) over time. Waveform 182 represents the magnitude of the process variable y(t) over time. From time t_0 to time t_A, tuning circuit 106 disturbs control output u(t), observes the measured process variable y(t), estimates the steady state control output U_{EST} and other process model parameters and then tunes the control parameters K_P and T_D, as discussed above. It should be understood that the tuning procedure and the tuning circuit 106 are optional with the present invention.

Adaptive tuning of bias value U_{RS} begins at time t_A. At time t_A, tuning circuit 106 provides the estimated steady state control output U_{EST} to ramp and hold circuit 126. PD controller 104 then begins controlling the process. As mentioned above, the estimated steady state control output U_{EST}, shown at 184, may be somewhat different than the real steady state control output U_{SS}, shown at 186.

At time t_{20}, the process variable y(t) reaches a stable state with a tracking error e_{SS} greater than e_{MAX}. A tracking error band of $2e_{MAX}$ is shown at 188 along waveform 182. At time t_{20}, bias value U_{RS} is updated to the real steady state control output U_{SS} with a ramp function, shown at 186. The process variable

$y(t)$ then reaches a new stable state 190 which has a tracking error e_{ss} that is less than e_{MAX}.

At time t_{21}, a disturbance or process load change occurs in process 112. PD controller 104 brings the process variable $y(t)$ to a new stable state, at 192, by varying control output $u(t)$. Since the stable state tracking error e_{ss} at 192 is greater than e_{MAX}, tracking error comparator circuit 130 closes switch 128 and updates bias reset value U_{RS} to equal the real control output steady state value U_{ss} with a ramp function, shown at 194. Process variable $y(t)$ reaches a new stable state, at 196, which has a tracking error e_{ss} that is less than e_{MAX}.

In an alternative embodiment, the adaptive bias value is added to the measured process variable $y(t)$ or the set point Y_{SET} as opposed to the control output signal $u(t)$. In this embodiment, the summing junction shown in Figure 3 is removed and an error bias value e_{BIAS} is added to summing junction 102. Equation 4 for PD control would therefore not include the term U_{RS}. The input of switch 128 is coupled to $e(t)$, as opposed to $u(t)$, to feed $e(t)$ back to ramp and hold circuit 126. The output of ramp and hold circuit 126 provides e_{BIAS} to summing junction 102. As a result summing junction 102 operates according to the following equation,

$$e(t) = Y_{SET} - y(t) + e_{BIAS} \qquad \text{Eq. 17}$$

In this case, the control goal is to force $y(t) = Y_{SET}$, that is $e(t) = e_{BIAS}$. At the steady state, $e(t) = e_{ss}$, $y(t) = Y_{ss}$. If e_{BIAS} is updated to equal e_{ss}, then, Y_{ss} is forced toward Y_{SET} in the above equation for the same reasons as were discussed with reference to Equation 8. The error bias value e_{BIAS} is updated in the same manner

as the bias value U_{RS} described above. It should be understood that the terms "add" and "sum" used herein includes adding positive or negative terms such that the addition may in fact be a subtraction.

Adaptive bias control eliminates the primary disadvantage of a lack of tracking ability in traditional P and PD control systems. The adaptive bias control of the present invention is simple, robust and adaptable for unexpected process disturbances and load changes. Since the adaptive bias control requires only simple calculations, it can be implemented in devices having limited power and memory, such as field mounted process control units. For example, a 4-20 mA current loop leaves only a few milliamps after the signal range is subtracted to power all of the electronic components in the unit. This limits the complexity of the components and the memory space that can be implemented in the unit. Typical memory transmitters available today are limited to 8K to 64K bytes, for example.

The adaptive bias control circuit of the present invention can also be implemented in a valve control unit, for example. Figure 6 is similar to Figure 2 and is a block diagram of a valve control unit 200 which includes input filter circuit 202, voltage regulator 204, adjustable current sink 206, current transducer 208, demodulator 210, A/D converter 212, modulator 214, microprocessor 216, memory 218, clock circuit 220, D/A converter 222 and actuator 224. Circuit 202, regulator 204, and current transducer 208 are connected in series with process control loop 226 for receiving the measured process variable y(t) and modulated digital data, such as a set point Y_{SET}, from the loop.

Demodulator 210 demodulates the data and provides the data to microprocessor 216 for analysis. Regulator 204 receives power from loop 226 and provides a regulated voltage for powering the elements of valve control unit 200. Current transducer 208 measures the analog current level y(t) in loop 226, which is converted by A/D converter 212 into digital data for microprocessor 216. Microprocessor 216 transmits data over loop 226 by modulating the current through sink 206 with modulator 214, such as by the HART® protocol. The auto-tuning algorithm, control algorithm, process model, tuning parameters and other user-defined constants are stored in memory 218 for configuring microprocessor 216 to control actuator 224 through D/A converter 222 as a function of the measured process variable y(t) and the set point Y_{SET}.

Although the present invention has been described with reference to preferred embodiments, workers skilled in the art will recognize that changes may be made in form and detail without departing from the spirit and scope of the invention. For example, the adaptive bias value can be added to the control output signal, the measured process variable or the set point value to move the tracking error e(t) toward zero. The adaptive bias control circuit can be implemented as a software routine or algorithm stored in memory for execution by a programmed computer, such as a microprocessor. In alternative embodiments, the circuit is implemented in digital or analog hardware. The control circuit can be located in the transmitter, in the valve or in master controller 10. Master controller 10 can be located in a central control room or at a remote location near the transmitter or valve. The control circuit can be used with any suitable tuning

circuit or method, such as the well known Ziegler-Nichols' open-loop tuning method, the modified Ziegler-Nichols' frequency domain (closed loop) method, or the method disclosed in the copending application referred to above. Alternatively, the present invention can be used without a tuning circuit.

WHAT IS CLAIMED IS:

1. A process control apparatus for controlling an integrating-type process based on a measured process variable and a set point, comprising:

error means for generating an error signal as a function of a comparison between the set point and the measured process variable;

non-integrating control means coupled to the error means for generating a first control signal as a function of the error signal; and

adaptive bias control means for adding a bias value to at least one of the first control signal, the measured process variable and the set point as a function of the error signal.

2. The process control apparatus of claim 1 wherein the adaptive bias control means includes means for monitoring the error signal and for selectively updating the bias value when an absolute value of the error signal exceeds a selected maximum error.

3. The process control apparatus of claim 2 wherein the means for selectively updating includes means for selectively updating the bias value according to a ramp function.

4. The process control apparatus of claim 2 wherein the adaptive bias control means is coupled to the non-integrating control means and includes means for generating a second control signal based on a sum of the first control signal and the bias value and wherein the means for selectively updating updates the bias value to equal the second control signal.

5. The process control apparatus of claim 2 wherein the adaptive bias control means is coupled to the error means and includes means for providing the bias signal to error means, wherein the error means generates the error signal based on a sum of the set point, the measured process variable and the bias value, and wherein the means for selectively updating updates the bias value to equal the error signal.

6. The process control apparatus of claim 1 wherein the adaptive bias control means comprises:

means for collecting N samples of the error signal and determining whether at least one of the N samples exceeds a selected maximum error;

means for fitting the N samples to a polynomial equation an + b, where a is the slope of the curve, b is the intercept and n is a variable representing the number of the sample;

means for updating the bias value when at least one of the N samples exceeds the selected maximum error and the absolute value of slope a is less than a selected maximum slope.

7. The process control apparatus of claim 6 wherein the adaptive bias control means further comprises:

means for updating the bias value to equal a sum of a past bias value and a selected integral gain constant K_i multiplied by intercept b when at least one of the N samples exceeds the selected maximum error, the absolute value of slope a is greater than a selected maximum slope

and a product of slope a and intercept b is greater than zero.

8. The process control apparatus of claim 1 wherein the adaptive bias control means comprises:

means for collecting N samples of the error signal and determining whether at least one of the N samples exceeds a selected maximum error;

means determining a variance in the N samples and for updating the bias value when at least one of the N samples exceeds the selected maximum error and the variance is less than a selected maximum variance.

9. A field-mounted control unit powered over a process control loop for controlling a process based on a measured process variable and a set point, comprising:

input-output means adapted to be coupled to the process control loop and for receiving power from the process control loop;

microprocessor means coupled to the input-output means and comprising:

error means having an input for receiving the measured process variable and the set point, wherein the error means generates an error signal as a function of a comparison between the measured process variable and the set point;

non-integrating control means coupled to the error means for generating a first control signal as a function of the error signal; and

adaptive bias control means for adding a bias value to at least one of the first control signal, the measured process variable and the set point as a function of the error signal; and

a memory coupled to the microprocessor means.

10. A process control system for controlling a process based on a measured process variable and a set point, comprising:

a process control loop;

a controller comprising:

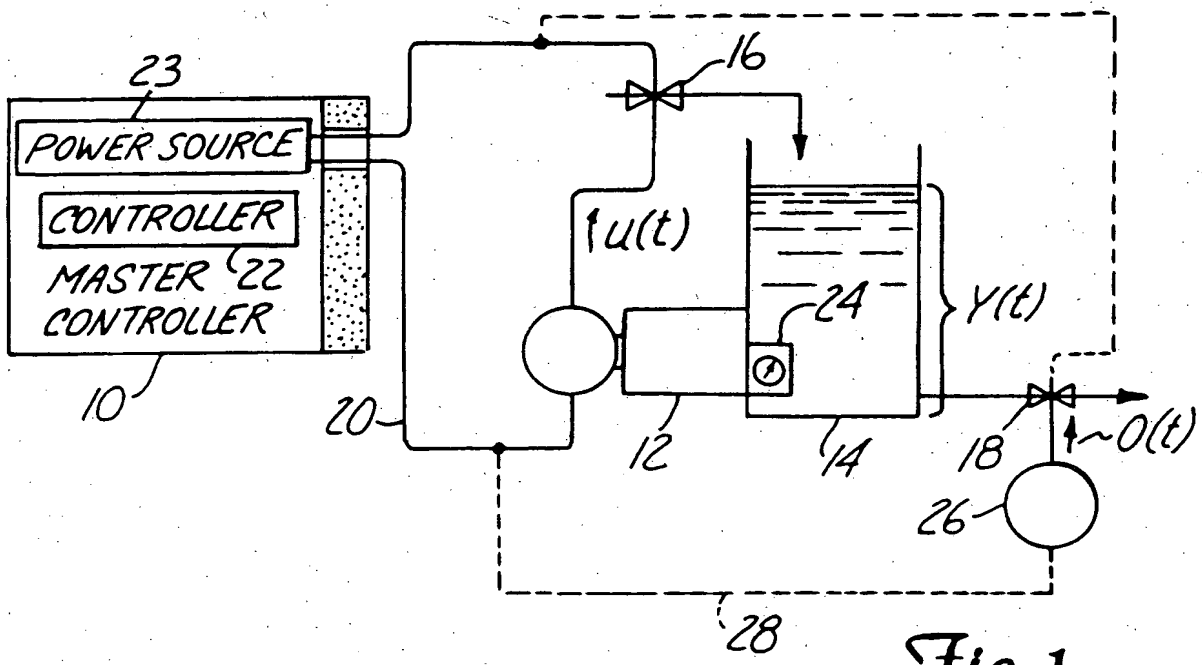
error means having an input for receiving the measured process variable and the set point, wherein the error means generates an error signal as a function of a comparison between the measured process variable and the set point;

non-integrating control means coupled to the error means for generating a control signal on the process control loop as a function of the error signal;

adaptive bias control means for adding a bias value to at least one of the control signal, the measured process variable and the set point; and

means for selectively updating the bias value as a function of the error signal; and

a field device coupled to the process control loop which controls the process as a function of the control signal.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POWER SOURCE
CONTROLLER
MASTER 22
CONTROLLER
10
16
u(t)
24
Y(t)
20
12
14
18
O(t)
26
28

Fig. 1

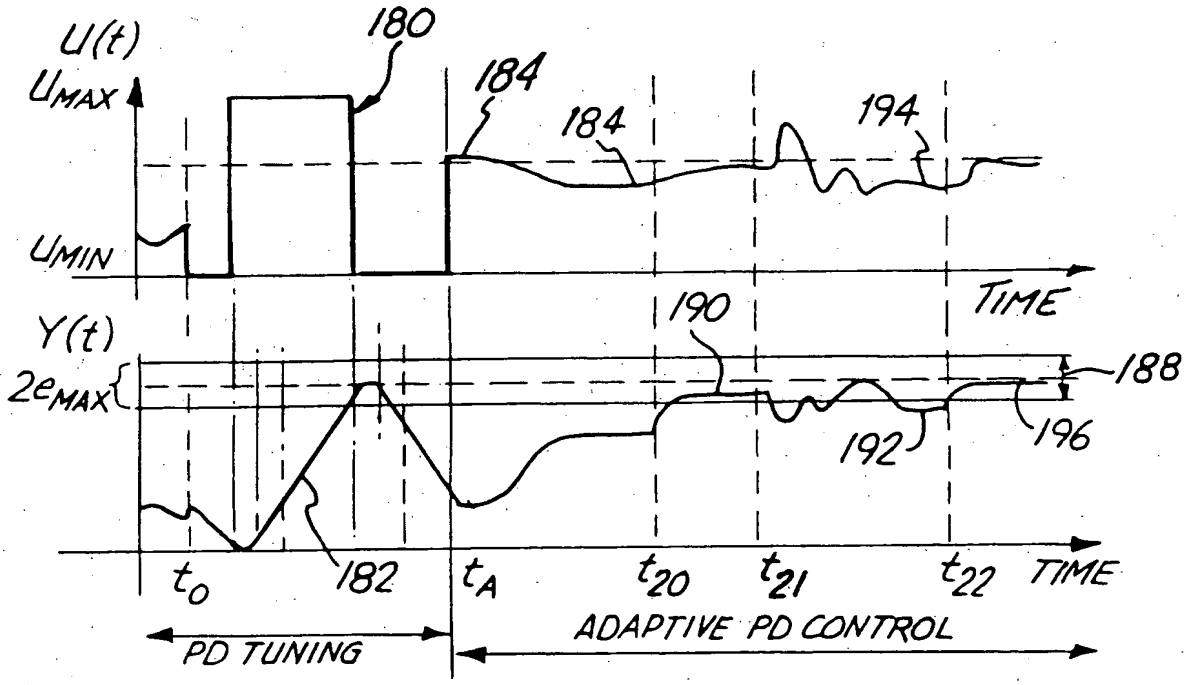
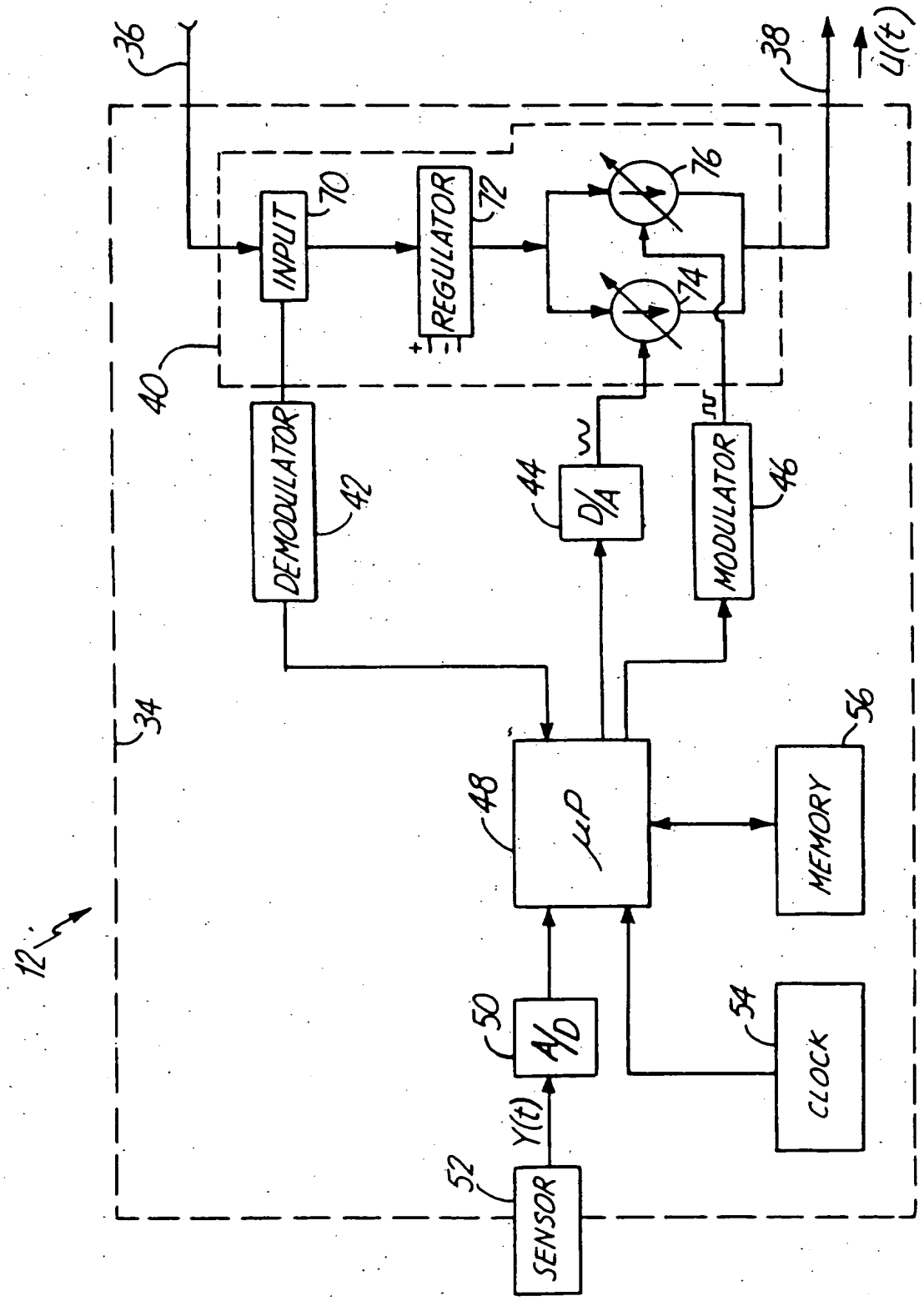

U(t)
180
184
184
194
UMAX
UMIN
TIME
Y(t)
190
188
2eMAX
192
196
t0
182
tA
t20
t21
t22
TIME
PD TUNING
ADAPTIVE PD CONTROL

Fig. 5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34
36
38
U(t)
40
INPUT
70
REGULATOR
72
74
76
DEMODULATOR
42
D/A
44
MODULATOR
46
μP
48
MEMORY
56
A/D
50
Y(t)
SENSOR
52
CLOCK
54

Fig. 2

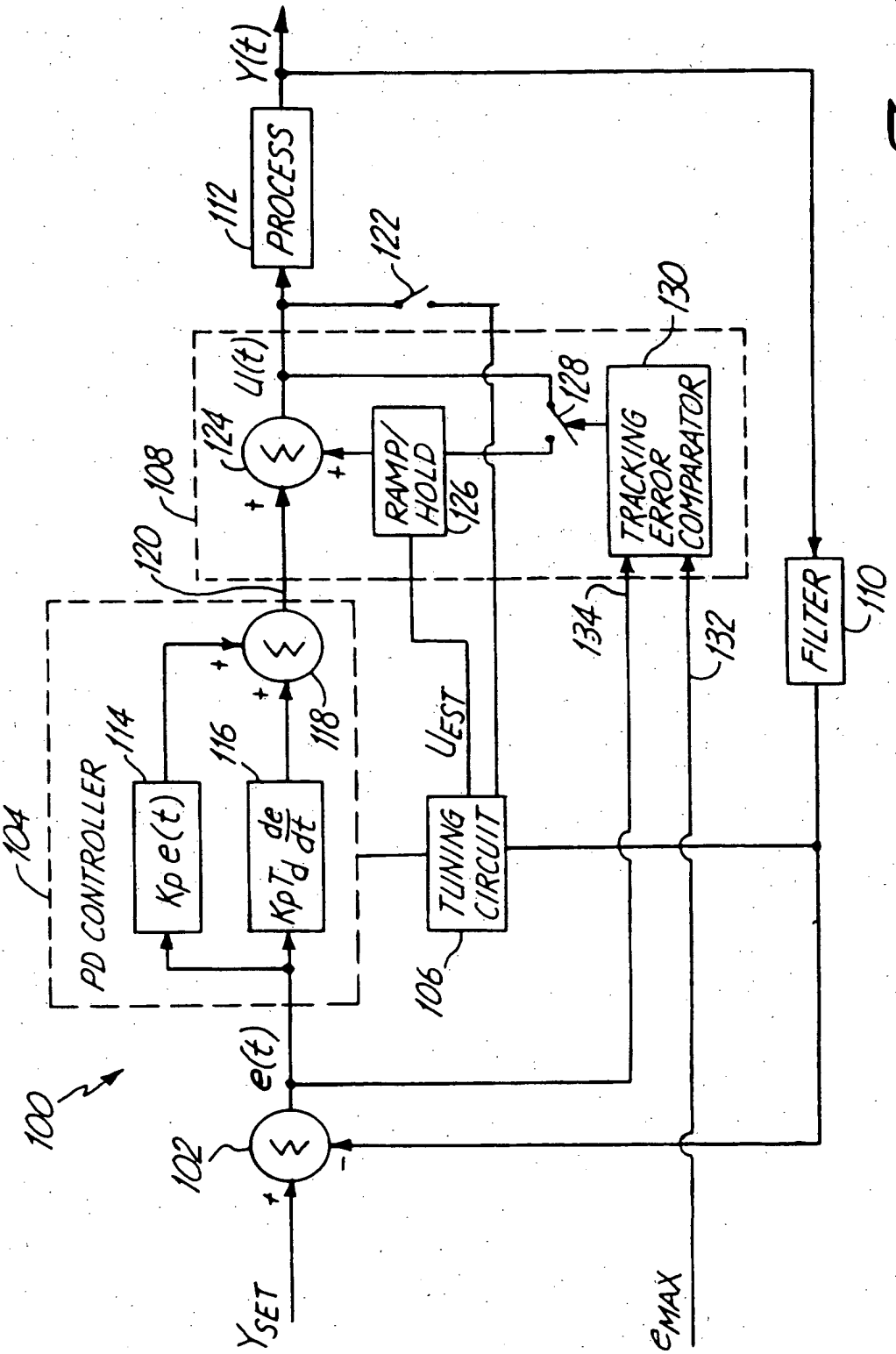
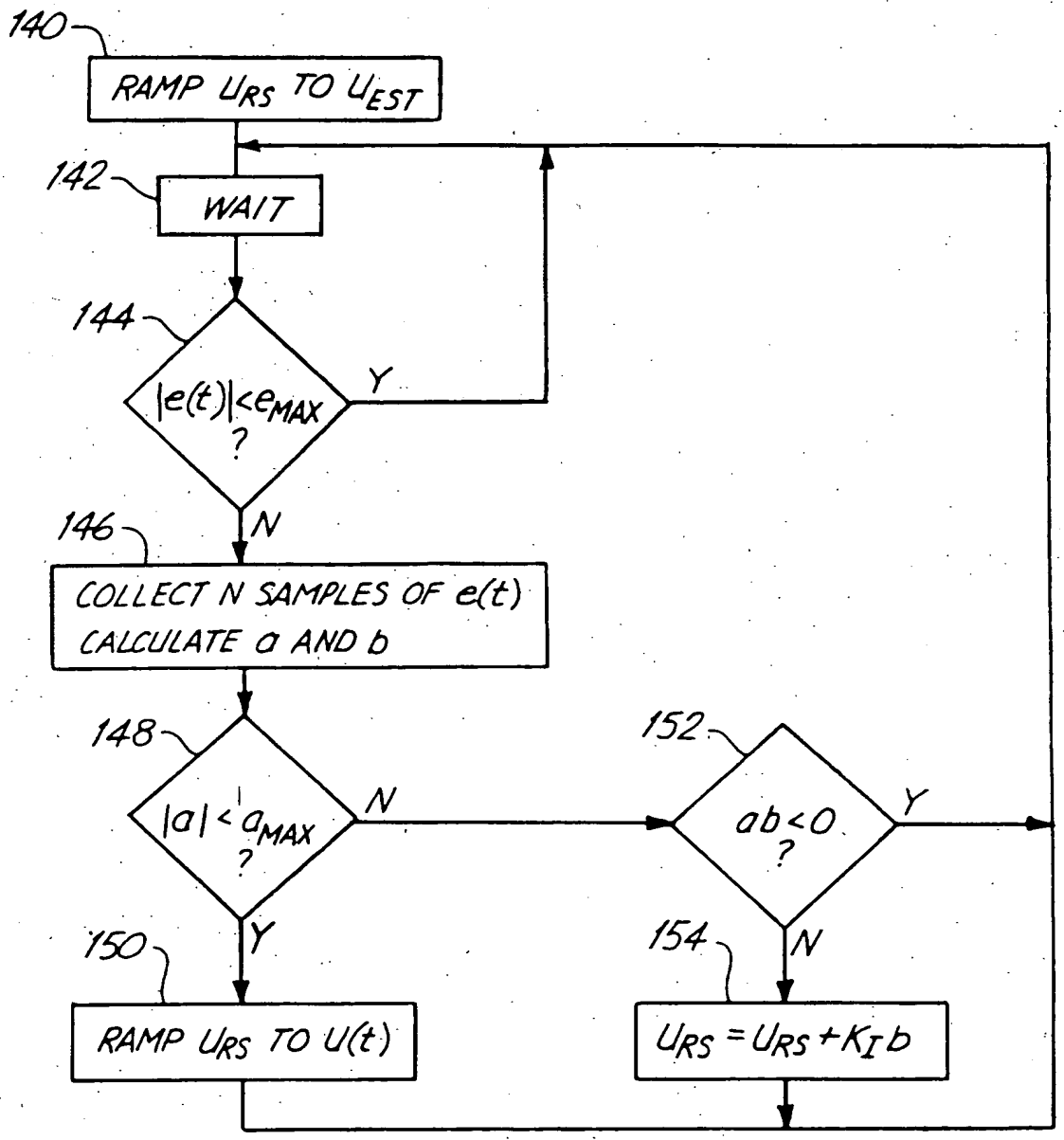

100
102
104
PD CONTROLLER
106
108
110
112
114
116
118
120
122
124
126
128
130
132
134
e(t)
Y(t)
U(t)
Y_{SET}
e_{MAX}
U_{EST}
$K_p e(t)$
$K_p T_d \frac{de}{dt}$
PROCESS
RAMP/ HOLD
TRACKING ERROR COMPARATOR
TUNING CIRCUIT
FILTER

Fig. 3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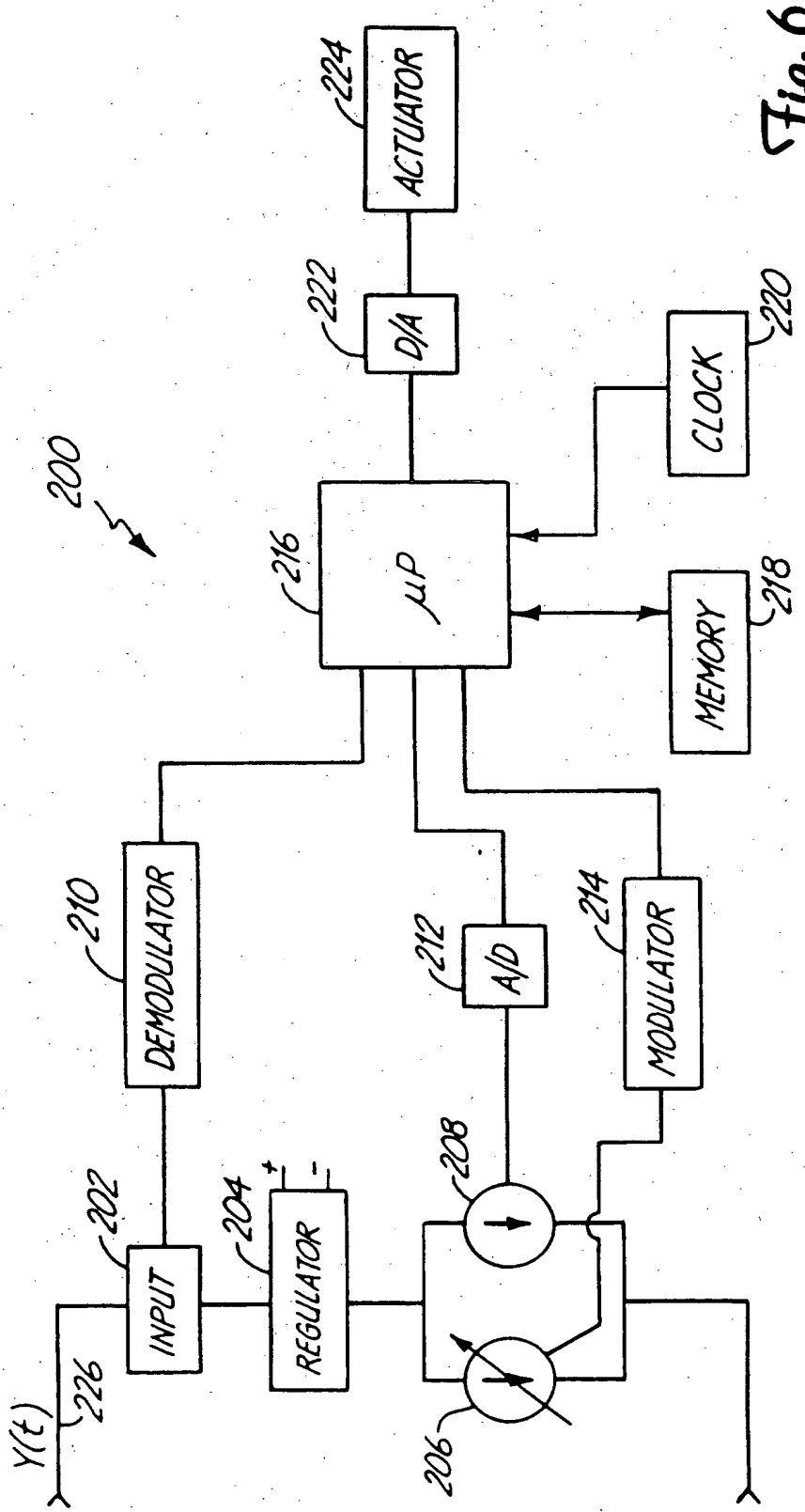
RAMP U_{RS} TO U_{EST}
142
WAIT
144
$|e(t)| < e_{MAX}$?
Y
N
146
COLLECT N SAMPLES OF e(t)
CALCULATE a AND b
148
$|a| < a_{MAX}$?
N
Y
150
RAMP U_{RS} TO U(t)
152
$ab < 0$?
Y
N
154
$U_{RS} = U_{RS} + K_I b$

Fig. 4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ACTUATOR
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D/A
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CLOCK
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μP
218
MEMORY
210
DEMODULATOR
212
A/D
214
MODULATOR
202
INPUT
204
REGULATOR
208
206
226
Y(t)

Fig. 6

INTERNATIONAL SEARCH REPORT

International Application No PCT/[redacted] 96/14509

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G05B11/42 G05B13/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP,A,0 260 987 (PIONEER ELECTRONIC CORP) 23 March 1988 see column 3, line 32 - column 4, line 56 ---	1,9,10
A	US,A,4 852 053 (TURRIE BRUCE D) 25 July 1989 see the whole document ---	1,9,10
A	US,A,5 278 478 (MOODY KRISTAAN L ET AL) 11 January 1994 see the whole document ---	1,9,10
A	EP,A,0 445 940 (TOKYO SHIBAURA ELECTRIC CO) 11 September 1991 see the whole document ---	1,9,10
	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 December 1996	14.01.97

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Kelperis, K

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 96/14509

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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1

INTERNATIONAL SEARCH REPORT

...on on patent family members

Inter...l Application No
PC... 96/14509

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